COMMUNICATION AND NETWORKING RISER ECR FORM

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Name of Originator: **Brad Barmore**

Company Name: **Intel Corporation**

Originator Contact Information:
Phone: (503) 696-4393
e-mail: brad.barmore@intel.com

Title of the Change: **Plug-and-Play EEPROM compliance and power supply requirement**

Specification Title and Version: **CNR Specification, Version 1.0**

Reason for Change:
There are many different styles of serial EEPROMs available on the market that could potentially be used as the CNR Plug-and-Play (PnP) EEPROM. This change clarifies the requirement by specifying that the PnP EEPROM must be compliant with the "System Management Bus Specification, Revision 1.1." In addition, the power supply requirement for the PnP EEPROM is clarified.

Description of Change:
Currently the CNR Specification does state that the PnP EEPROM be connected to the +3.3VD power supply (Section 4.1.4) and that it be compliant with the "System Management Bus Specification, Revision 1.1" (Section 6.1.1.1). The changes below update and further reinforce those requirements by high-lighting appropriate text, and also repeating the requirements in the rules for claiming CNR compliance. Each of these changes are shown below in red.

4.1.4 SMBus Interface Power Management

Power management for the SMBus interface is very straightforward. Since the BIOS only reads the contents of the SMBus EEPROM (electrically erasable programmable read only memory) during ACPI state S0, one can make the valid assumption that the +3.3VD power supply is sufficient for power the SMBus EEPROM. In fact, if the CNR board designer follows this specification, which requires the SMBus PnP EEPROM be fully compliant with the System Management Bus Specification, Revision 1.1 (dated December 11, 1998), there will not be any issues (as the System Management Bus Specification, Revision 1.1, requires that the leakage current on an unpowered SMBus device be less than 5uA). However, to ensure that the SMBus interface is not excessively loaded while the system is in a sleep state it is strongly recommended that the SMBus EEPROM be powered by the +3.3Vdual power supply (pin A18 of both the Type A and Type B connectors).

~~The power management for the SMBus interface is very straightforward. The system must be in ACPI state S0, or a full working state, since the SMBus EEPROM (electrically erasable programmable read only memory) is only accessed at boot time by the BIOS. This implies that all power supplies are available. Thus the SMBus EEPROM should be connected to the +3.3VD power supply, to ensure that it is functional only when the system is in a full working state.~~

6.1.1.1 Plug and Play EEPROM Device Considerations

In general, SMBus EEPROM devices are available in a variety of memory sizes and addressing capabilities. Care must be taken by the designer of the CNR board to select an EEPROM device that is fully addressable and is large enough to store the required data. The following is a list of the specific requirements for the PnP EEPROM device.

1. The PnP EEPROM device **must** be compatible with the System Management Bus Specification, Revision 1.1 (dated December 11, 1998). Note that compliance to the future versions of the System Management Bus Specification may cause hardware incompatibilities, until SMBus Controllers supporting the specification releases are widely available.

Add the following additional CNR rules to Section 8:

7. The SMBus Plug-and-Play EEPROM device **must** be compliant with the System Management Bus Specification, Revision 1.1 (dated December 11, 1998).